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Noise Shaping All Digital Phase

The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion. Readers will gain a deep understanding of ADPLLs and the central role played by noise-shaping.

Amazon.com: Noise-Shaping All-Digital Phase-Locked Loops ...

This book presents a novel approach to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping. Realistic examples illustrate how to analyze and simulate phase noise in the presence of sigma-delta modulation and time-to-digital conversion.

Noise-Shaping All-Digital Phase-Locked Loops: Modeling ...

Noise-Shaping All-Digital Phase-Locked Loops: Modeling, Simulation, Analysis and Design (Analog Circuits and Signal Processing) 2014th Edition. by Francesco Brandonisio (Author), Michael Peter Kennedy (Author) ISBN-13: 978-3319036588. ISBN-10: 3319036580. Why is ISBN important?

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Noise-Shaping All-Digital Phase-Locked Loops : Modeling, Simulation, Analysis and Design by Francesco Brandonisio and Michael Peter Kennedy. This book presents a novel approach to the analysis and design of all-digital phase-locked loops (ADPLLs), technology widely used in wireless communication devices. The authors provide an overview of ADPLL architectures, time-to-digital converters (TDCs) and noise shaping.

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An all-digital phase locked loop (ADPLL) generally comprises a digitally controlled oscillator (DCO), a digital loop filter that applies a multiple bit control word to the DCO, a digital adder with...

US20070205931A1 - All-digital phase locked loop (adpll ...

Second and Third-Order Noise Shaping Digital Quantizers for Low Phase Noise and Nonlinearity-Induced Spurious Tones in Fractional-N PLLs Eythan Familiar, Member, IEEE, and Ian Galton, Fellow, IEEE Abstract—Noise shaping digital quantizers, most commonly digital delta-sigma ($\Delta\Sigma$) modulators, are used in fractional-N phase-locked loops (PLLs) to enable fractional frequency tuning.

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In a conventional ADC, an analog signal is sampled with a sampling frequency and subsequently quantized in a multi-level quantizer into a digital signal. This process introduces quantization error noise. The first step in a delta-sigma modulation is delta modulation.

Delta-sigma modulation - Wikipedia

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